=always horny 3= verilog What does always block * means? Stack Overflow Verilog Always block using * symbol Stack.

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The * means build the sensitivity list for me. For example if you had a statement a = b + c then you d want a to change every time either b or c changes. In other words a is sensitive to b c

So to set this up always b or c begin a = b + c end But imagine you had a largealwaysblock that was sensitive to loads of signals. Writing the sensitivity list would take ages. In fact Thealways * syntax was added to the IEEE Verilog Std in 2001. All modern Verilog tools simulators synthesis etc

support this syntax. Here is a quote from the LRM 1800 2009 An incomplete event_expression list of an event control is a common source of bugs in register transfer level RTL simulations

The implicit event_expression * is a convenient shorthand that eliminates these Mar 12 2012 So alwaysuse always * or better yet always_comb and forget about the concept of sensitivity lists. If the item in the code is evaluated it will trigger the process. Simple as that

It an item is in an if else a case assigned to a variable or anything else it will be evaluated and thus cause the process to be triggered Sep 25 2015 always * was added by Verilog IEEE 1364 2001 standard and replaced byalways_comb in the SystemVerilog IEEE 1800 2005 standard.always * should no longer be used because it does not correctly simulate hardware in all cases

In addition to the difference you note with functions it does not handle constant logic correctly. parameter C = 0 reg A B always * A = B C A remains Apr 16 2014 I am totally confused among these 4 terms always_ff always_comb always_latch andalways

How and for what purpose can these be used? Jan 14 2012 The expressionalways * begin name_of_my_combinational_logic_block code end describes combinational logic

Typically the clk and rst signals are not read from inside of this type ofalwaysblock so they don t appear in the sensitivity list like wisemonkey says

It is best practice to use * for the sensitivity lists of combinational logic so that you don t forget to include a signal Apr 11 2013 The difference between forever andalwaysis thatalwayscan exist as a module item which is the name that the Verilog spec gives to constructs that may be written directly within a module not contained within some other construct

initial is also a module item.alwaysblocks are repeated whereas initial blocks are run once at the start of Aug 16 2013 The point of the .done .fail .always methods is that you can Attach multiple handlers Do so anywhere and not just

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